PCI Bus Target Interface Megafunction

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Target Application:
Buses & Interfaces

Family:
FLEX 10K & FLEX 8000

Vendor:

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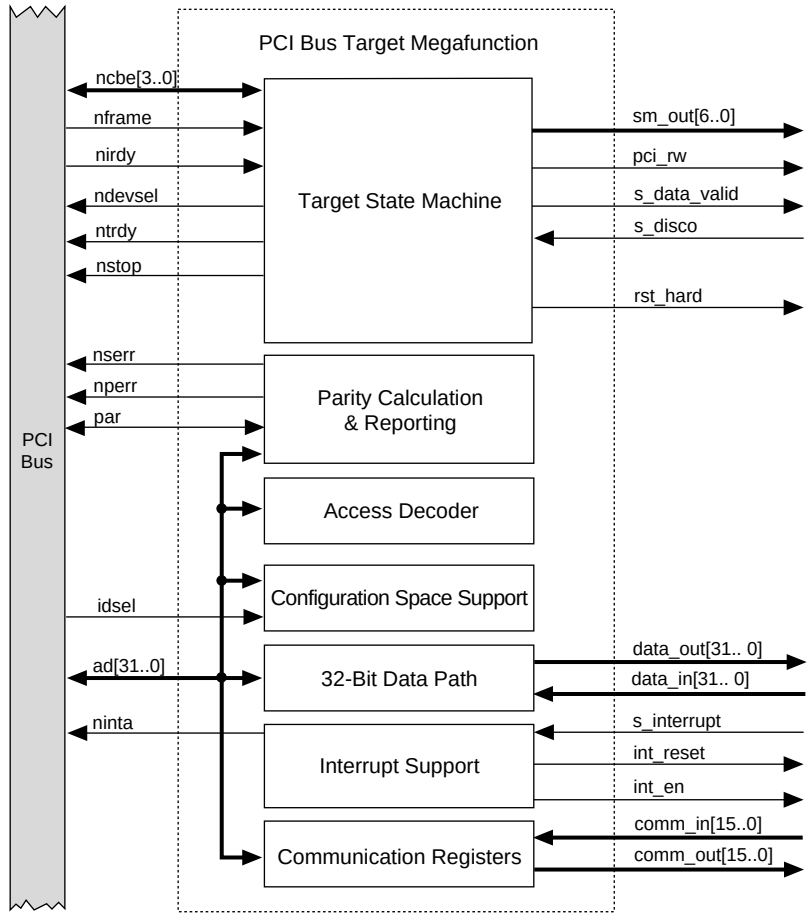
Features

- Optimized for the Altera® FLEX® 10K and FLEX 8000 device architectures
- Fully compliant with peripheral component interconnect Special Interest Group (PCI-SIG) ***PCI Local Bus Specification***, Rev. 2.1
- Fully synchronous design
- Fully hardware tested
- Supports full-speed burst support up to 132 Mbytes/second
- Provides zero-wait state data transfer rate

General Description

The PCI bus target interface megafunction is a 32-bit PCI bus interface that is used for high-speed data transfers and real-time computing applications such as fast data-intensive projects and migration of ISA-based designs to PCI bus designs. Figure 1 shows a block diagram of the megafunction.

Figure 1. PCI Bus Target Interface Megafunction Block Diagram



Functional Description

The PCI bus target interface megafunction provides a simple and flexible interface between a PCI bus and a user-developed back-end application. The megafunction maintains high performance and accuracy through full parity calculation and reporting. PCI bus handling is implemented with full support for disconnect and retry events; the megafunction handles one interrupt.

Performance

The PCI bus target interface megafunction operates at 33 MHz. Table 1 provides the typical utilization results for the megafunction.

Table 1. Typical Utilization Results for the PCI Bus Target Interface Megafunction

Implementation	Target Device	Clock (f_{MAX})	EABs	Logic Cells	% of Logic Cells Used
32-bit PCI bus target	EPF10K10-3	33 MHz	0 / 3	340 / 576	60%
	EPF10K20-3	33 MHz	0 / 6	340 / 1152	30%
	EPF10K30-3	33 MHz	0 / 6	340 / 1728	20%
	EPF10K40-3	33 MHz	0 / 8	340 / 2304	15%
	EPF10K10-3	33 MHz	3 / 3	340 / 576	80%
32-bit PCI bus target with internal SRAM	EPF10K20-3	33 MHz	4 / 6	450 / 1152	40%
	EPF10K30-3	33 MHz	4 / 6	450 / 1728	25%
	EPF10K40-3	33 MHz	4 / 8	450 / 2304	20%

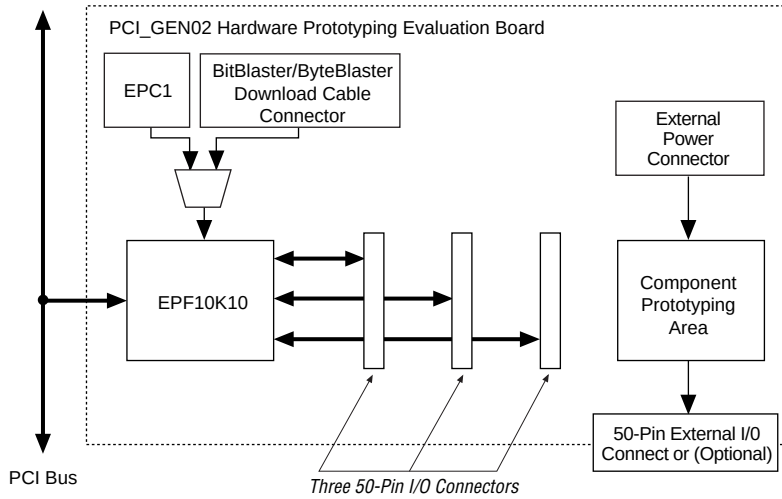
Customization

The PCI bus target interface megafunction is fully parameterizable, allowing the designer to customize the memory space location and size (between 16 bytes and 64 Mbytes), and the device, vendor, class code, and revision ID registers.

Hardware Testing

The PCI bus target interface megafunction has been developed and tested using the PCI_GEN02 PCI bus evaluation board (available from PLD Applications). The PCI_GEN02 contains an EPF10K10 device that implements the megafunction. The megafunction uses only 60% of the EPF10K10 device, the remaining logic and EAB resources are available for user-defined custom logic. Figure 2 shows a block diagram of the PCI_GEN02 PCI bus evaluation board.

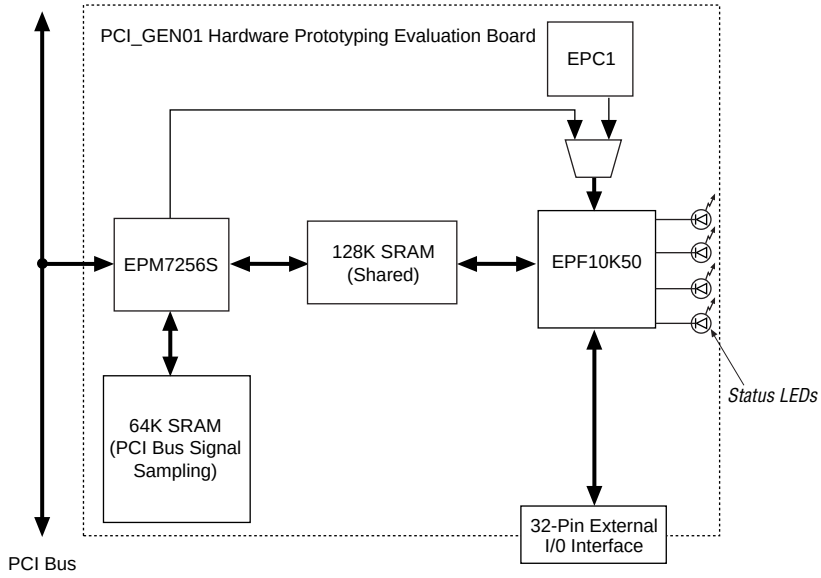
Figure 2. Block Diagram of the PCI_GEN02 PCI Bus Evaluation Board



The EPF10K10 device can be configured using an EPC1™ Configuration EPROM, a BitBlaster™ download cable, or a ByteBlaster™ download cable. These options allow the designer to choose between a variety of configuration techniques. Three 50-pin headers are provided for a daughter card, and a 50-pin off-card connector is supported by the PCI_GEN02 solder mask.

PCI bus target applications can also be developed and tested using the PCI_GEN01 PCI bus evaluation board. The PCI_GEN01 is used to implement custom hardware on the PCI bus. The PCI_GEN01 contains an EPM7256S device that implements the PCI target interface and an EPF10K50 device that is used for user-defined custom logic. The EPF10K50 device can be configured using an EPC1 Configuration EPROM or via the PCI target interface. Figure 3 shows a block diagram of the PCI_GEN01 PCI bus evaluation board.

Figure 3. Block Diagram of the PCI_GEN01 PCI Bus Evaluation Board



The EPF10K50 device provides significant logic resources for implementing and evaluating hardware on the PCI bus. The EPM7256S and EPF10K50 devices share a common 128-Kbyte SRAM space. The EPM7256S device controls a separate 64-Kbyte SRAM buffer that captures PCI bus control signals and provides a signal analyzer for the PCI bus. The EPF10K50 device drives the four status LEDs, and it is connected to an external 32-pin I/O interface.

Reference

PCI Special Interest Group. ***PCI Local Bus Specification***. Rev.2.1 Hillsboro, Oregon: PCI Special Interest Group, 1995.

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